noise will be forced to escape to the power lines 8B, 9B through the input protection circuit 3BB, and then is discharged to the outside from the lower power terminal 5B and the ground terminal 6B, and also propagates and diffuses across the internal circuit 4B. In this event (see two-dot chain lines and so on in Fig. 12C), the difference between a time required for the surge noise to reach the active element 12BP in the first connection configuration through the power line 8B and a time required for the surge noise to reach the active element 12BN in the first connection configuration through the power line 9B cannot be ignored. In addition, it is also contemplated that an element which has been intensively and locally affected by the difference in potential with the inter-circuit signal wire 12 has also become more susceptible to failure.

IN THE CLAIMS:

Please amend the claims as follows:

1. (Amended Twice) A semiconductor integrated circuit device comprising:

a plurality of internal circuits arranged internally in a circuit forming region, said internal circuits having different power lines;

an inter-circuit signal wire arranged to interconnect said internal circuits, wherein said inter-circuit signal wire is not directly connected to an input circuit or an output circuit; and

a plurality of active elements in a second connection configuration including

elements of an identical or similar structure to an active element in a first connection configuration connected to said inter-circuit signal wire,

said plurality of active elements in said second connection configuration being arranged adjacent to said active element in the first connection configuration to sandwich or surround said active element in the first connection configuration,

said plurality of active elements in said second connection configuration being connected to power lines of said internal circuits associated therewith and being isolated from signal wires other than said inter-circuit signal wire.

2. (Amended Twice) A semiconductor integrated circuit device according to claim 1, wherein each of said internal circuits includes a plurality of basic cells regularly arranged in repetition, and said active element in the first connection configuration and said plurality of active elements in the second connection configuration are allocated to some of said basic cells.

5. (Amended Twice) A semiconductor integrated circuit device comprising:

a plurality of internal circuits arranged internally in a circuit forming region, said internal circuits having different power lines;

an inter-circuit signal wire arranged to interconnect said internal circuits, wherein said inter-circuit signal wire is not directly connected to an input circuit or an output circuit; and

an active element in a second connection configuration arranged adjacent to an active element in a first connection configuration connected to said inter-circuit signal wire, including

an element of an identical or similar structure to said active element in the first connection configuration,

said active element in a second connection configuration being connected to power lines of said internal circuits associated therewith and being isolated from said inter-circuit signal wire and other signal wires.

7. (Amended) A semiconductor integrated circuit device according to claim 5, wherein each of said internal circuits includes a plurality of basic cells regularly arranged in repetition,

and said active element in the first connection configuration and said plurality of active elements in the second connection configuration are allocated to some of said basic cells.

10. (Amended Twice) A semiconductor integrated circuit device according to claim 5, further comprising an active element in a third connection configuration, arranged adjacent to said active element in the first connection configuration and including an element of an identical or similar structure to said active element in the first connection configuration, said active element in the third connection configuration being connected to a power line of an internal circuit associated therewith and said inter-circuit signal wire and being isolated from other signal lines.

15. (Amended Twice) A semiconductor integrated circuit device according to claim 10, wherein:

a plurality of said inter-circuit signal wires having different communication directions from each other are arranged to interconnect a pair of internal circuits;

said active element in the second connection configuration and said active element in the third connection configuration are arranged adjacent to said active element in the first connection configuration on a reception side of said inter-circuit signal wire in one of said pair of internal circuits; and

said active elements in the third connection configuration are arranged independent of said active element in the second connection configuration, near said active element in the first connection configuration on a reception side of said inter-circuit signal wire in the other one of said pair of internal circuits.